

University of California, Santa Barbara
 Department of Electrical and Computer Engineering

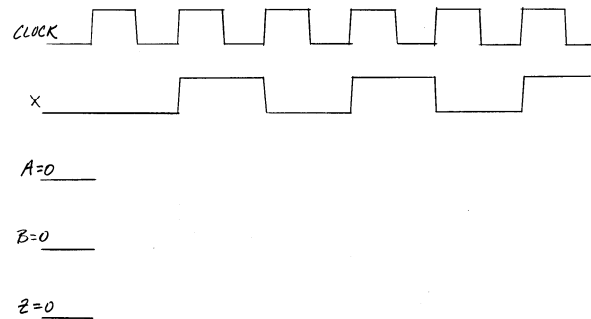
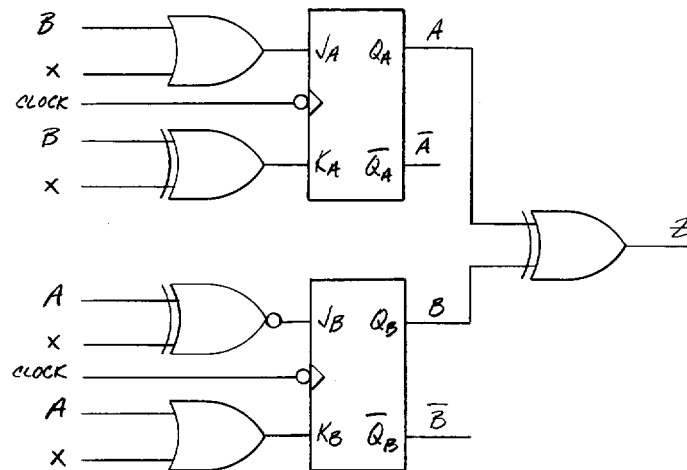
ECE 152A – Digital Design Principles

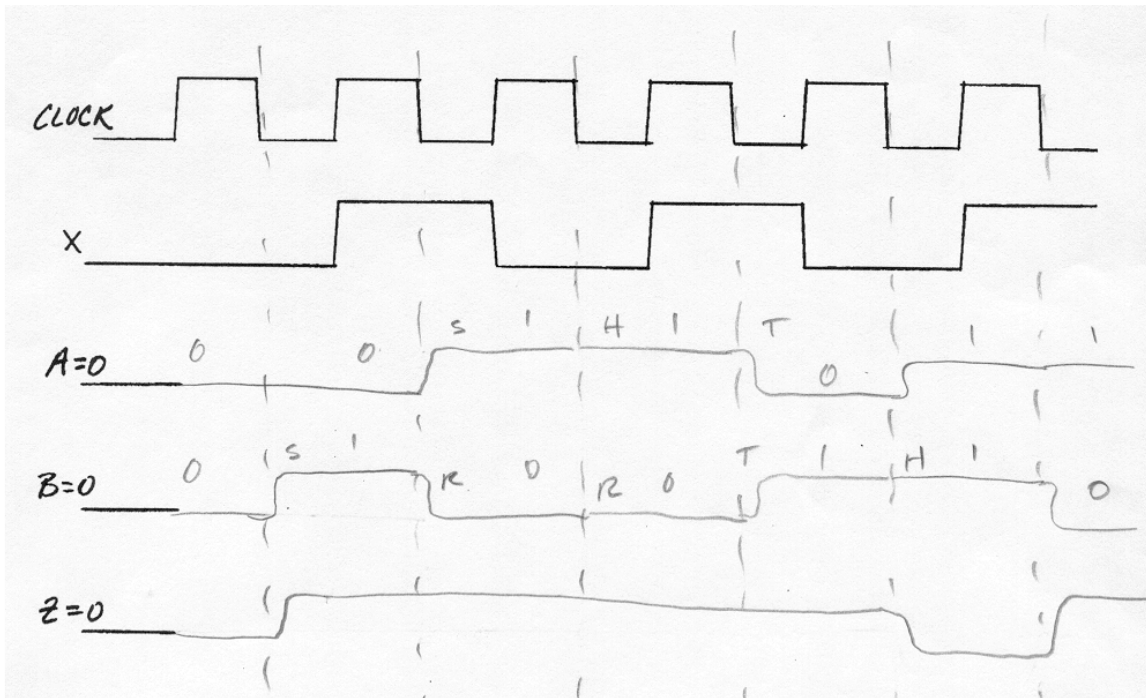
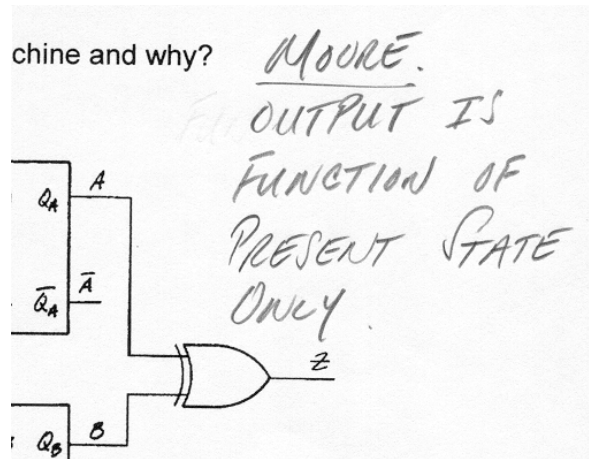
Homework #5 – Solution

Problem #1.

For the logic diagram below, complete the timing diagram. You can assume the gate delays are much shorter than the clock period.

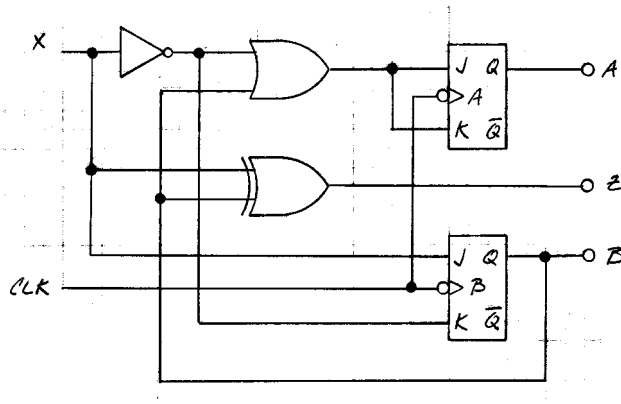
Is this a Mealy machine or a Moore machine and why?





Problem #2.

For the network shown below:



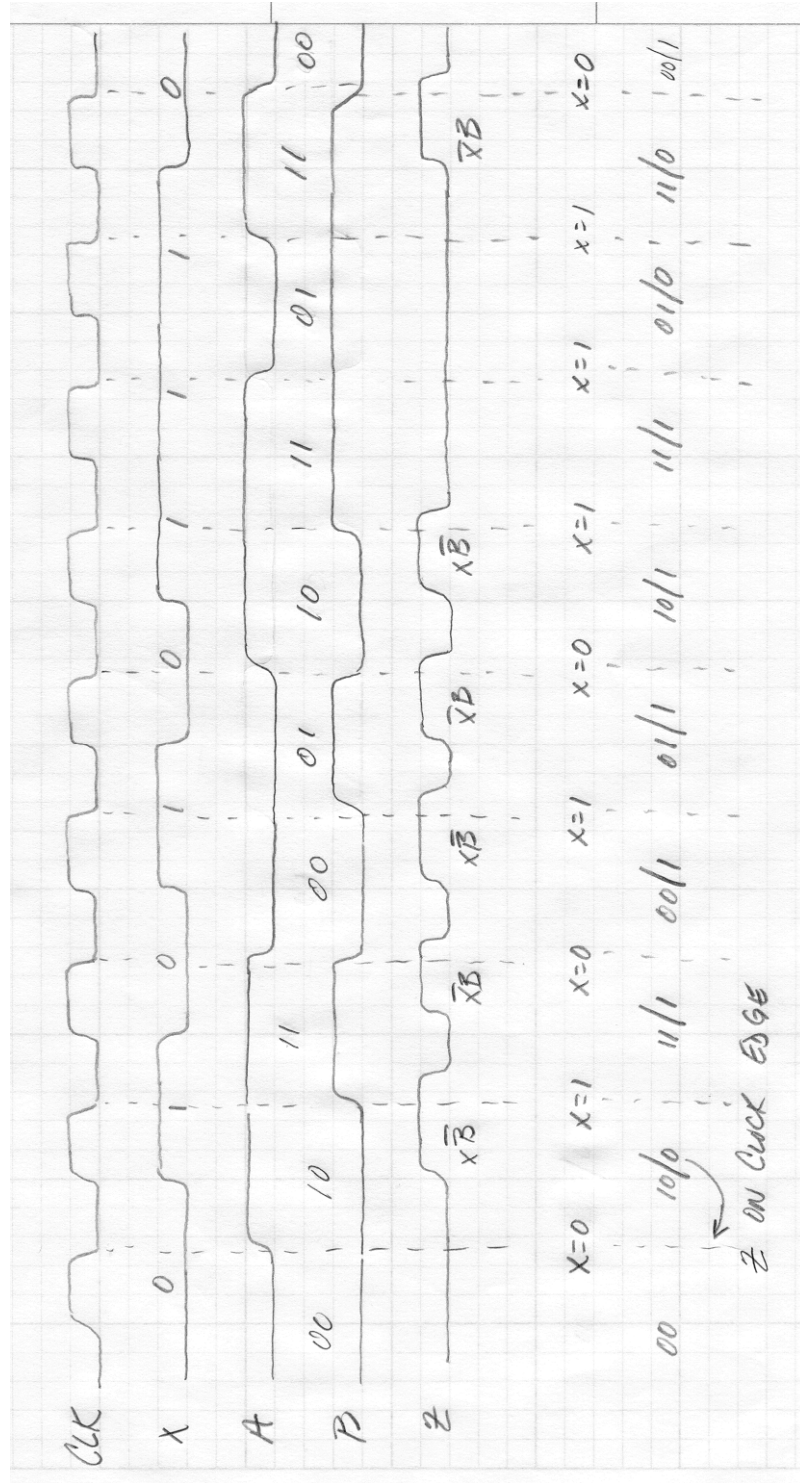
1. Construct a timing diagram for the input sequence:

$$X = 010101110$$

Assume that:

- 1) X, A and B are all initially equal to 0
- 2) All transitions of the input X occur on the rising edge of the clock
- 3) gate delays are much shorter than the clock period.

Include all inputs (CLK, X) state variables (A, B) and outputs (Z) in your timing diagram.



		AB			
X		00	01	11	10
0		1	1	X	X
1		0	1	X	X

$J_A = \bar{X} + B$

		AB			
X		00	01	11	10
0		X	X	1	1
1		X	X	1	0

$K_A = \bar{X} + B$

		AB			
X		00	01	11	10
0		0	X	X	0
1		1	X	X	1

$J_B = X$

		AB			
X		00	01	11	10
0		X	1	1	X
1		X	0	0	X

$K_B = \bar{X}$

		AB			
X		00	01	11	10
0		0	1	1	0
1		1	0	0	1

$Z = X\bar{B} + \bar{X}B$

		AB			
X		00	01	11	10
0		1	1	0	0
1		0	1	0	1

A^+

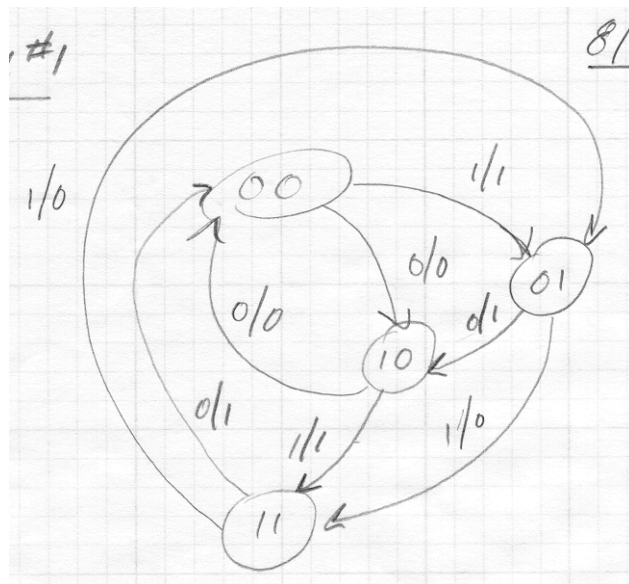
		AB			
X		00	01	11	10
0		0	0	0	0
1		1	1	1	1

B^+

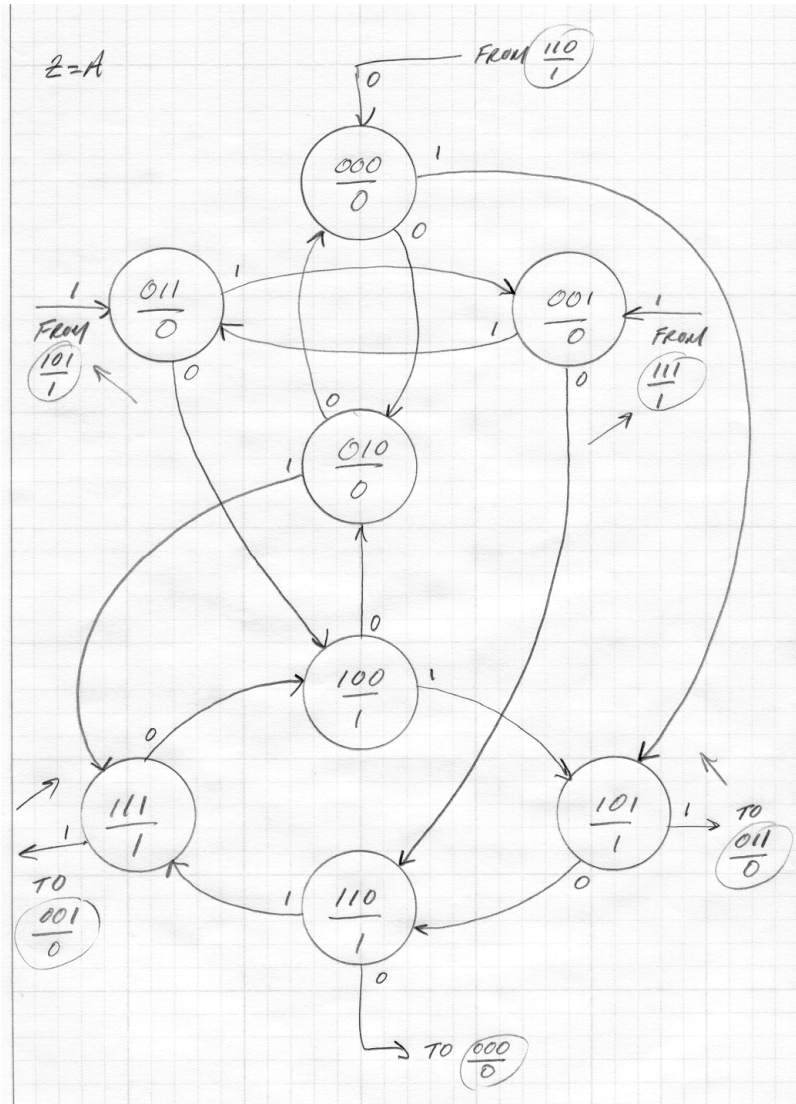
3. Construct the state table for the network.

A	B	$A+B^+$		Z	
		X=0	X=1	X=0	X=1
0	0	10	01	0	1
0	1	10	11	1	0
1	0	00	11	0	1
1	1	00	01	1	0

4. Construct the state diagram for the network



5. Redesign the network as a Moore machine. Include a state diagram, state table, next state maps and flip flop input maps. Implement your design with negative edge triggered JK flip flops.



PS			NS			z			
A	B	C	x=0	x=1					
0	0	0	0	1	0	1	0		
0	0	1	1	1	0	0	1	0	
0	1	0	0	0	0	1	1	0	
0	1	1	1	0	0	0	0	1	0
1	0	0	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0	1	1

xA	BC			
	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$A^+ = \bar{x}C + x\bar{C}$

xA	BC			
	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	1	0	1
10	0	1	0	1

$$B^+ = \bar{x}\bar{B} + \bar{B}C + xB\bar{C}$$

xA	BC			
	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$$C^+ = X$$

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

xA	BC			
	00	01	11	10
00	0	1	1	0
01	X	X	X	X
11	X	X	X	X
10	1	0	0	1

$$J_A = \bar{x}C + x\bar{C}$$

xA	BC			
	00	01	11	10
00	X	X	X	X
01	1	0	0	1
11	0	1	1	0
10	X	X	X	X

$$K_A = xC + \bar{x}\bar{C}$$

xA	BC			
	00	01	11	10
00	1	1	X	X
01	1	1	X	X
11	0	1	X	X
10	0	1	X	X

$$J_B = \bar{x} + C$$

xA	BC			
	00	01	11	10
00	X	X	1	1
01	X	X	1	1
11	X	X	1	0
10	X	X	1	0

$$K_B = \bar{x} + C$$

XA	BC				XA	BC			
	00	01	11	10		00	01	11	10
00	0	X	X	0	00	X	1	1	X
01	0	X	X	0	01	X	1	1	X
11	1	X	X	1	11	X	0	0	X
10	1	X	X	1	10	X	0	0	X

$J_c = X$ $K_c = \bar{X}$

$Z = A$

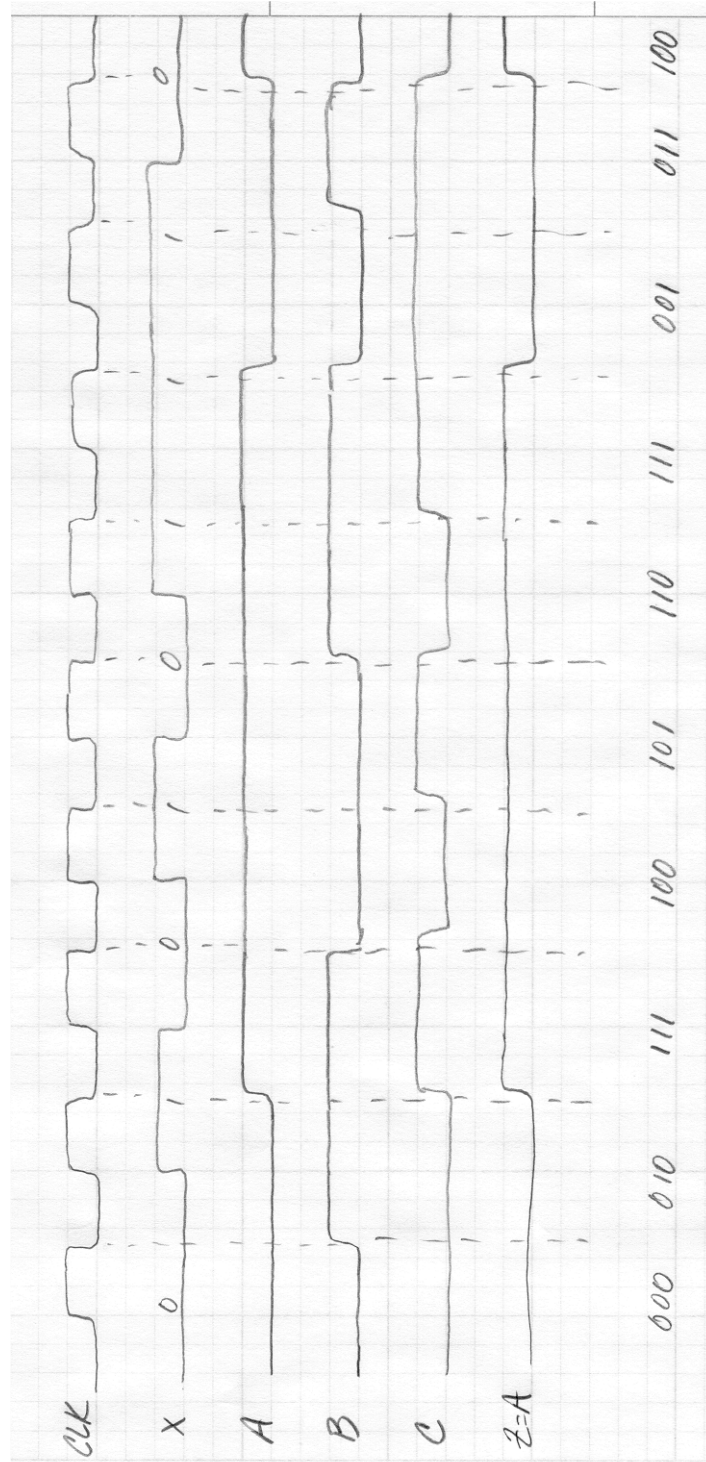
6. For the Moore machine designed in part 5, construct a timing diagram for the input sequence:

$$X = 0\ 1\ 0\ 1\ 0\ 1\ 1\ 1\ 0$$

As in part 1, assume that:

- 1) X, A and B are all initially equal to 0
- 2) All transitions of the input X occur on the rising edge of the clock
- 3) gate delays are much shorter than the clock period.

Include all inputs (CLK, X) state variables (A, B) and outputs (Z) in your timing diagram.



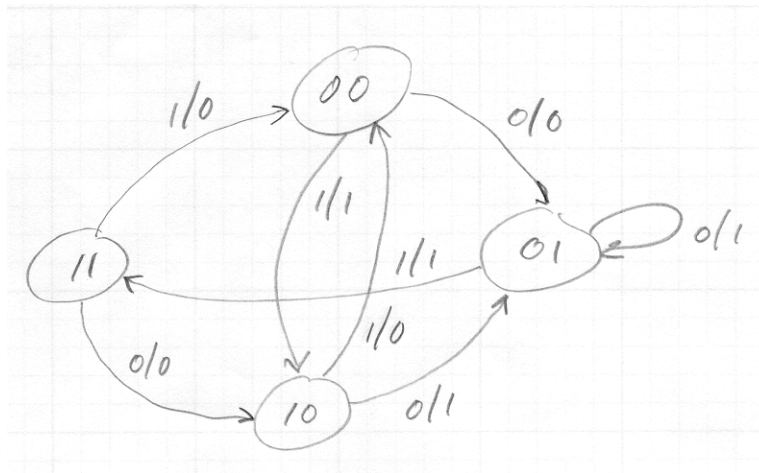
Problem #3.

A Mealy machine is defined by the following state table:

PS	NS,z
----	------

AB	x=0	x=1
00	01,0	10,1
01	01,1	11,1
10	01,1	00,0
11	10,0	00,0

1. Construct the state diagram for the Mealy machine.



2. Assuming that 00 is the initial state, determine the sequence of states and outputs in response to the input sequence:

$0 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 0 \rightarrow 1 \rightarrow 1$

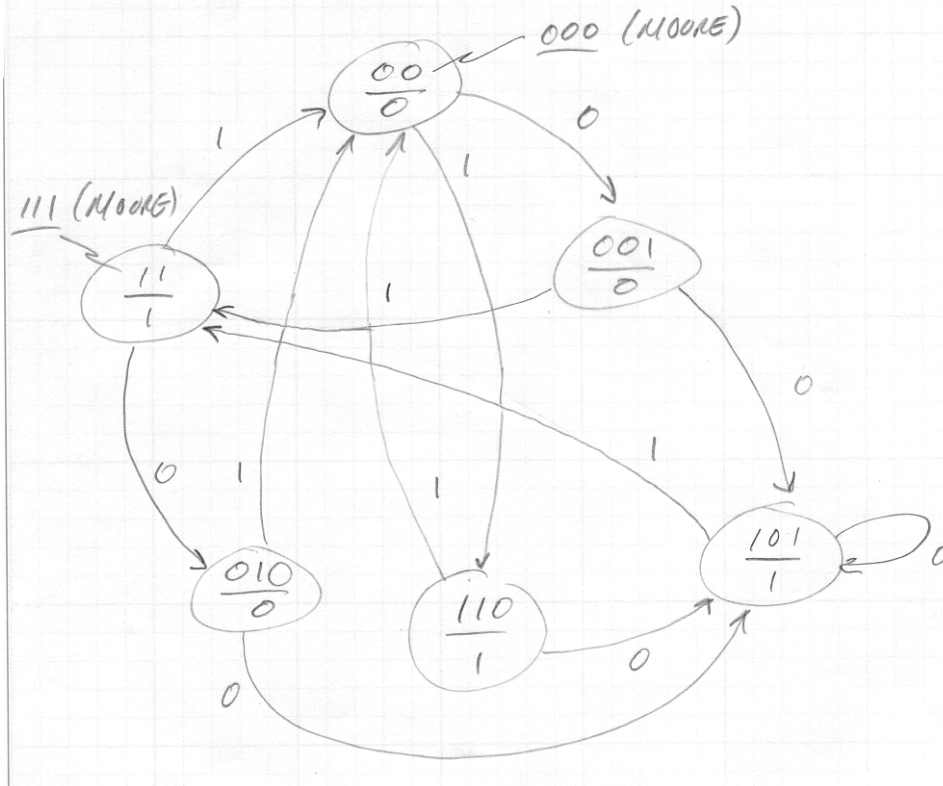
X =	0	0	1	0	0	1	1
NS =	01	01	11	10	01	11	00
Z =	0	1	1	0	1	1	0

3. Construct the state diagram for the equivalent Moore machine.

3. SPLIT STATES 01 AND 10

$$01 \rightarrow 001 + 101$$

$$10 \rightarrow 010 + 110$$



4. Construct a state table for the equivalent Moore machine.

PS	NS		z
	x=0	x=1	
0 0 0	0 0 1	1 1 0	0
0 0 1	1 0 1	1 1 1	0
0 1 0	1 0 1	0 0 0	0
0 1 1	x x x	x x x	x
1 0 0	x x x	x x x	x
1 0 1	1 0 1	1 1 1	1
1 1 0	1 0 1	0 0 0	1
1 1 1	0 1 0	0 0 0	1

5. Demonstrate that the machines are equivalent by applying the same input sequence as applied to the Mealy machine:

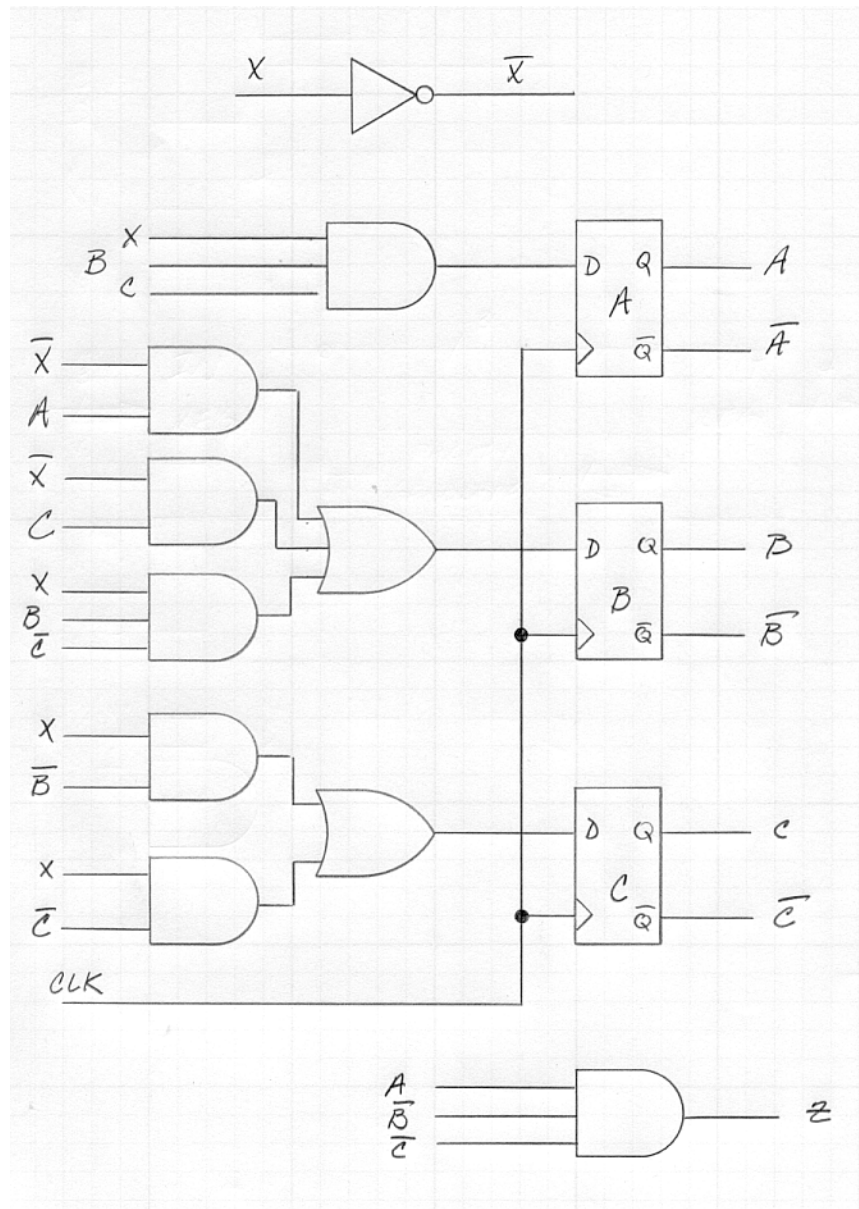
$0 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 0 \rightarrow 1 \rightarrow 1$

and observing the same output sequence. Identify both the sequence of states and the sequence of outputs (The state sequence will be different, but the output sequence should be the same).

x =	0	0	1	0	0	1	1
NS =	001	101	111	010	101	111	000
z =	0	1	1	0	1	1	0

Problem #4.

Consider the state machine below having a single input x , a single output z and three state variables, A , B and C :



1. Is this a Mealy machine or a Moore machine (and why)?

IT'S A MOORE MACHINE BECAUSE THE OUTPUT IS A FUNCTION OF PRESENT STATE ONLY

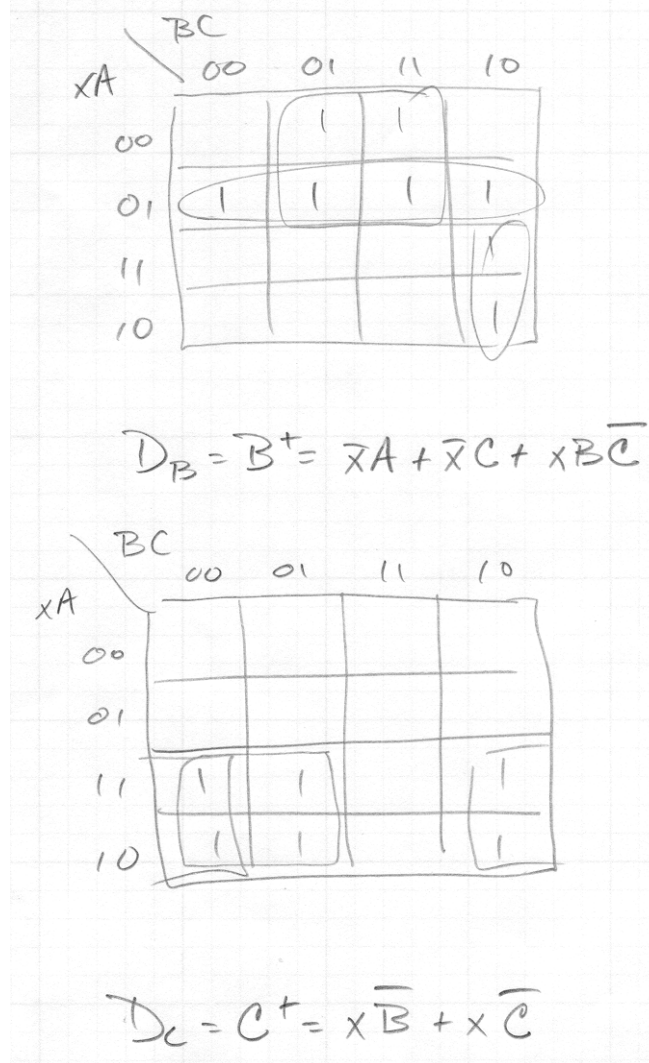
2. From the logic diagram, construct next state maps for the three state variables (A, B and C)

NEXT STATE MAPS

BECAUSE $D = Q^+$, WE CAN MAP THE D INPUTS DIRECTLY ONTO THE NEXT STATE MAPS

BC	00	01	11	10
XA				
00				
01				
11			1	
10			1	

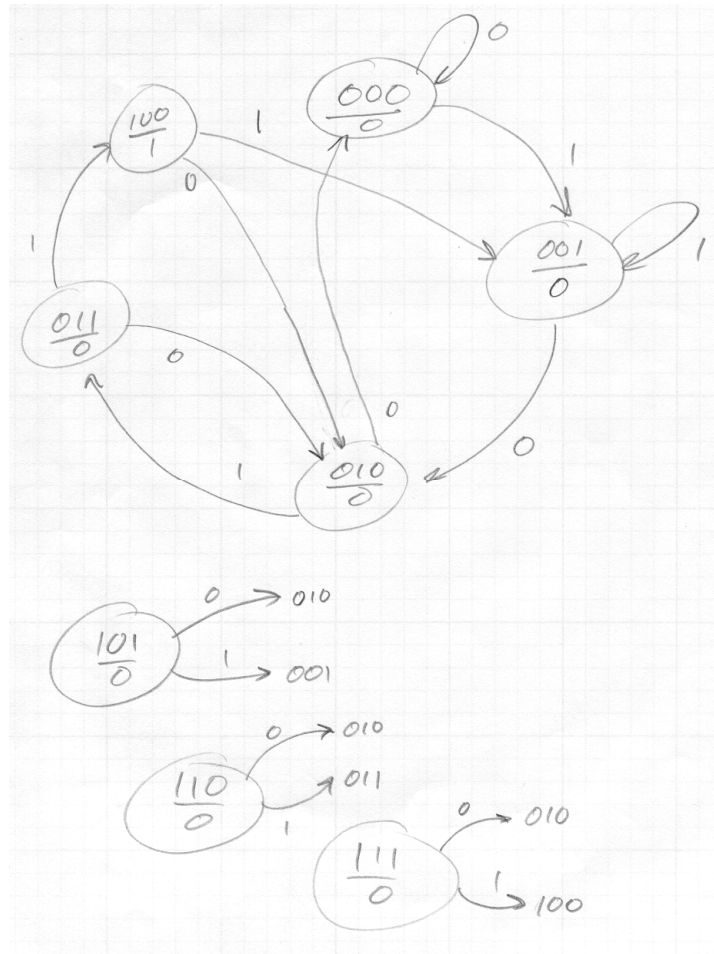
$$D_A = A^+ = xBC$$



3. From the next state maps, construct a state table. Include both the next state and output information.

PS			x=0			x=1			z
A	B	C	A ⁺	B ⁺	C ⁺	A ⁺	B ⁺	C ⁺	
0	0	0	0	0	0	0	0	1	0
0	0	1	0	1	0	0	0	1	0
0	1	0	0	0	0	0	1	1	0
0	1	1	0	1	0	1	0	0	0
1	0	0	0	1	0	0	0	1	1
1	0	1	0	1	0	0	0	1	0
1	1	0	0	1	0	0	1	1	0
1	1	1	0	1	0	1	0	0	0

4. From the state table construct the state diagram. Include the output information on the state diagram as is appropriate for this type of machine.



5. This state machine implements a sequence detector. The output z goes high when the correct sequence has been detected. Based on the state diagram and assuming that 000 is the initial state, what is the "correct" input sequence?

FROM INITIAL STATE 000

1 0 1 1

RESULTS IN OUTPUT = 1 IN STATE 100